intel®

PRELIMINARY

8XC196KB/8XC196KB16
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

- **8 Kbytes of On-Chip ROM/OTP Available**
- **232 Byte Register File**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **1.75 µs 16 x 16 Multiply (16 MHz)**
- **3.0 µs 32/16 Divide (16 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **12 MHz and 16 MHz Available**
- **Dedicated 15-Bit Baud Rate Generator**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **Pulse-Width-Modulated Output**
- **Four 16-Bit Software Timers**
- **10-Bit A/D Converter with Sample/Hold**
- **$\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol**
- **Extended Temperature Available**

The 8XC196KB is a 16-bit microcontroller available in three different memory varieties: ROMless (80C196KB), 8K ROM (83C196KB) and 8K OTP (One Time Programmable-87C196KB). The 8XC196KB is a high performance member of the MCS® 96 microcontroller family. The 8XC196KB has the same peripheral set as the 8096BH and has a true superset of the 8096BH instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 80C196KB. With a 16 MHz oscillator a 16-bit addition takes 0.50 µs, and the instruction times average 0.37 µs to 1.1 µs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 8XC196KB has a maximum guaranteed frequency of 12 MHz. The 8XC196KB16 has a maximum guaranteed frequency of 16 MHz. All references to the 80C196KB also refer to the 80C196KB16; 83C196KB, Rxxx; 87C196KB and 87C196KB16 unless otherwise noted. The ROM device does not have a speed indicator at the end of the device name. Instead it has a ROM code number.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

*Other brands and names are the property of their respective owners.

July 2004 Order Number: 270909-007

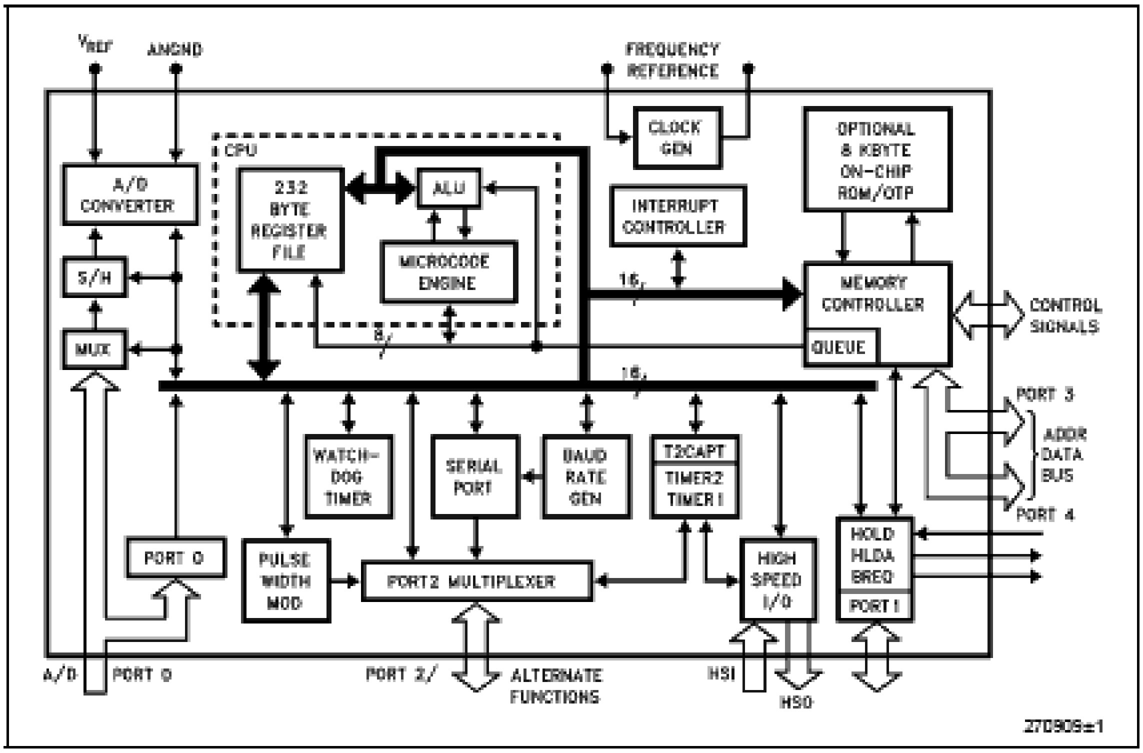
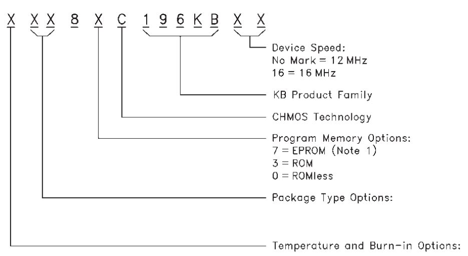


Figure 1. 8XC196KB Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0 and 629.1, a CHMOS III-E process. Additional process and reliability information is available in the *Intel® Quality System Handbook:* http://developer.intel.com/design/quality/quality.htm



NOTE: 270909–2
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XC196KB Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196KB Memory Map

Description	Address
External Memory or I/O	0FFFFH 04000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	3FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H. (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEH
External Memory	1FFDH 0100H
232 Bytes Register RAM (Note 1)	00FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 00FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KB quick reference for SFR descriptions.
5. WARNING: Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

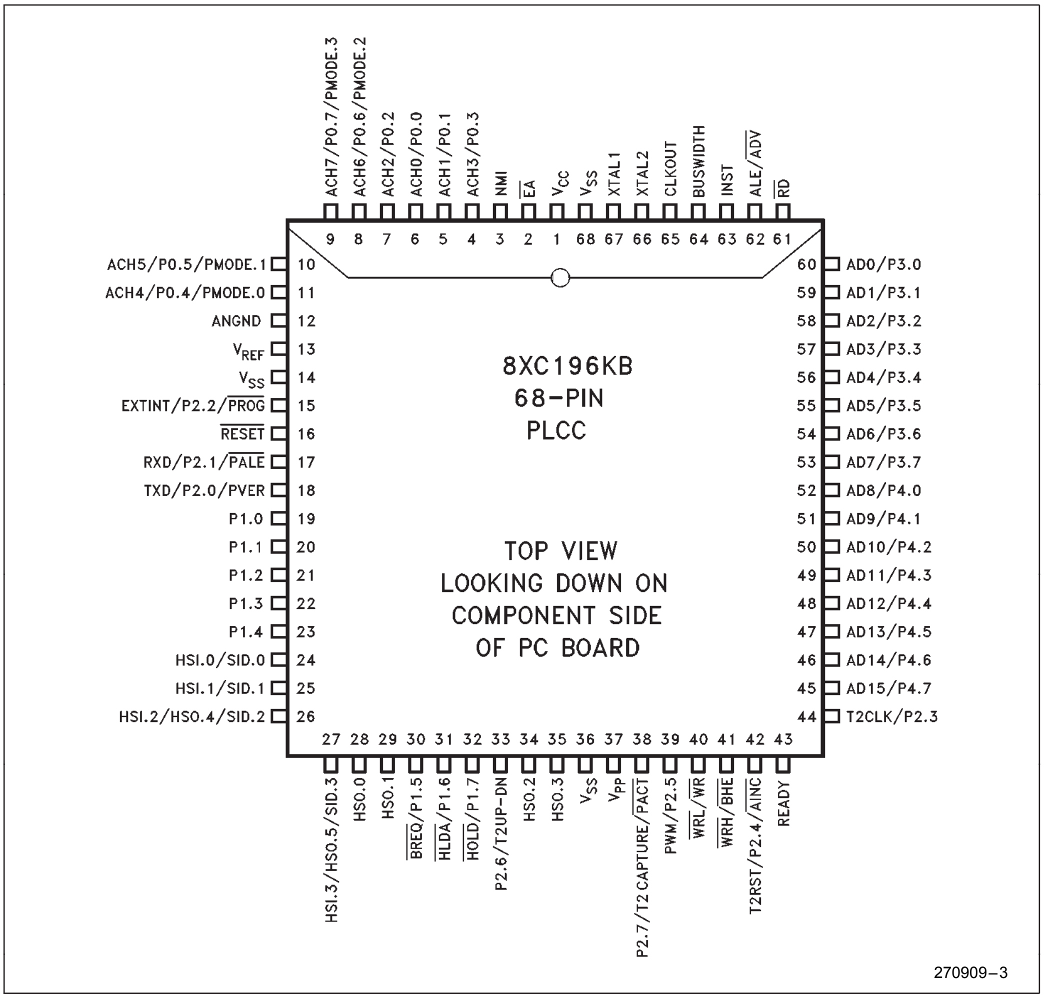
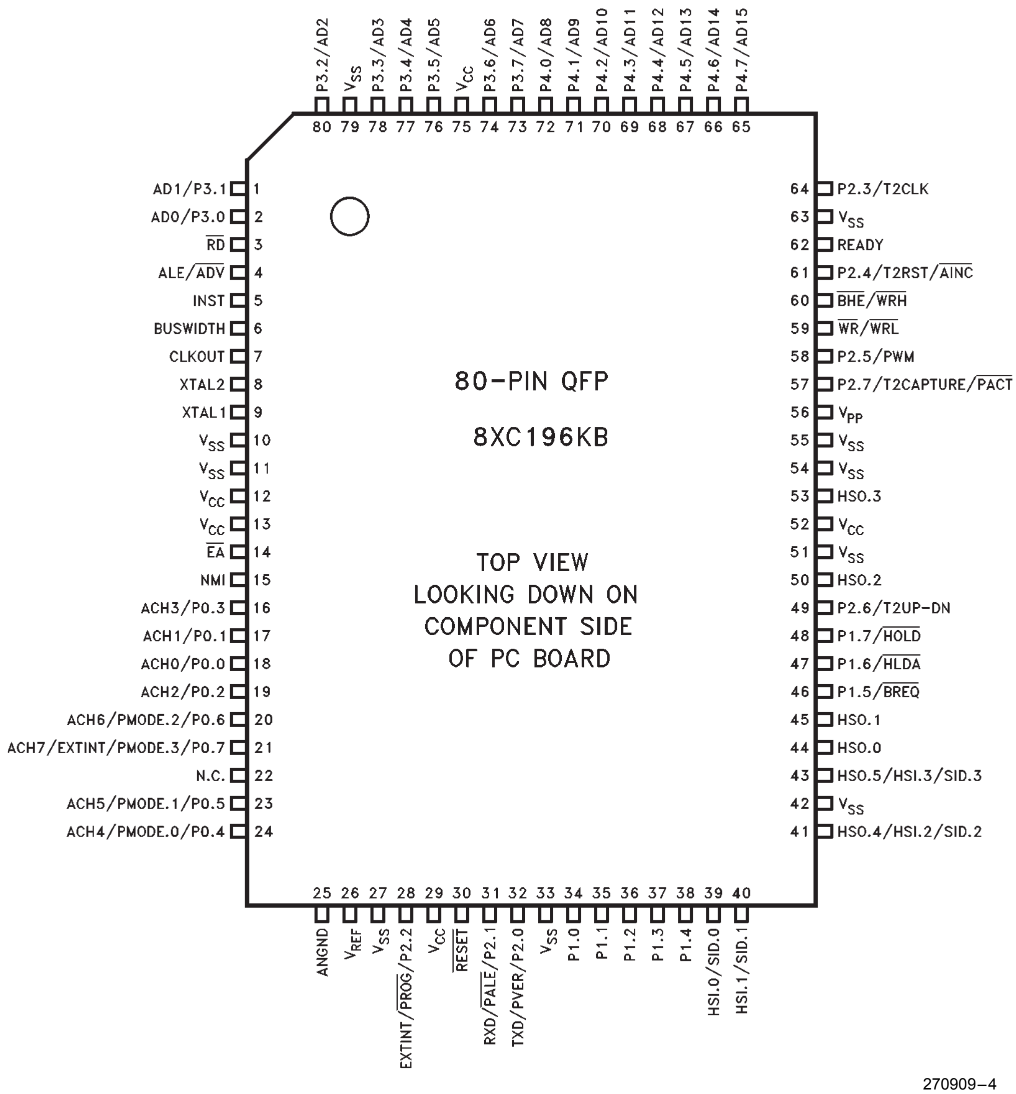


Figure 3. 68-Pin Package (PLCC Top View)

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: AINC, PALE, PMODE.n, and PROG. The ROMless (80C196KB) doesn't use any of the programming pins.



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 4. 80-Pin QFP Package

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: AINC, PALE, PMODE.n, and PROG. The ROMless (80C196KB) doesn't use any of the programming pins.

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}. Connect V_{SS} and ANGND at chip to avoid noise problems.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/OTPR OM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being addressed. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB. Pins P2.6 and P2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus, which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In Mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In Mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The pulse width modulator output.
T2UP-DN	The T2UPDN pin controls the direction of Timer2 as an up or down counter.
T2CAPTURE	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
Ports 3 and 4 (Programming Mode)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} when used in slave programming mode.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias................................. −55°C to +125°C

Storage Temperature.................... −65°C to +150°C

Voltage On Any Pin to V_{SS}................ −0.5V to +7.0V

Power Dissipation(1)..........................1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING*: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency 12 MHz	3.5	12	MHz
F_{OSC}	Oscillator Frequency 16 MHz	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (All Pins except XTAL1 and RESET)	$0.2\ V_{CC} + 0.9$	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage on XTAL 1	$0.7\ V_{CC}$	$V_{CC} + 0.5$	V	
V_{IH2}	Input High Voltage on RESET	2.6	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	$I_{OL} = 200\ \mu A$ $I_{OL} = 3.2\ mA$ $I_{OL} = 7\ mA$
V_{OH}	Output High Voltage (Standard Outputs)(2)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V V V	$I_{OH} = -200\ \mu A$ $I_{OH} = -3.2\ mA$ $I_{OH} = -7\ mA$
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)(1)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V V V	$I_{OH} = -10\ \mu A$ $I_{OH} = -30\ \mu A$ $I_{OH} = -60\ \mu A$
I_{LI}	Input Leakage Current (Std. Inputs)(3)		±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)		+3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)(1)		−800	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)(1)		−50	μA	$V_{IN} = 0.45V$

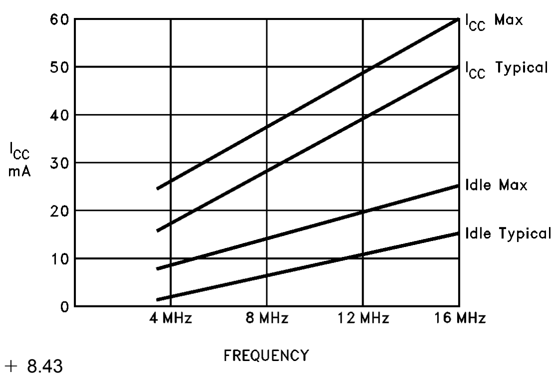
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
I_{IL1}	Logical 0 Input Current in Reset $\overline{BHE}$, $\overline{WR}$, P2.0			−850	μA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current in Reset ALE, $\overline{RD}$, INST			−7	mA	V_{IN} = 0.45V
I_{IH1}	Logical 1 Input Current on NMI Pin			100	μA	V_{IN} = 2.0V
Hyst.	Hysteresis on RESET Pin	300			mV	
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz V_{CC} = V_{PP} = V_{REF} = 5.5V
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{PD}	Powerdown Mode Current		5	30	μA	V_{CC} = V_{PP} = V_{REF} = 5.5V
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES: (Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0±15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0±AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST±CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and V_{REF} = V_{CC} = 5V.



I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

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Figure 6. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The system must meet these specifications to work with the 87C196KB:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2 T_{OSC} - 75$	ns	
T_{YLYH}	NonREADY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2 T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2 T_{OSC} - 75$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3 T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2 T_{OSC} \times n$ where n = number of wait states.

AC CHARACTERISTICS (Continued)

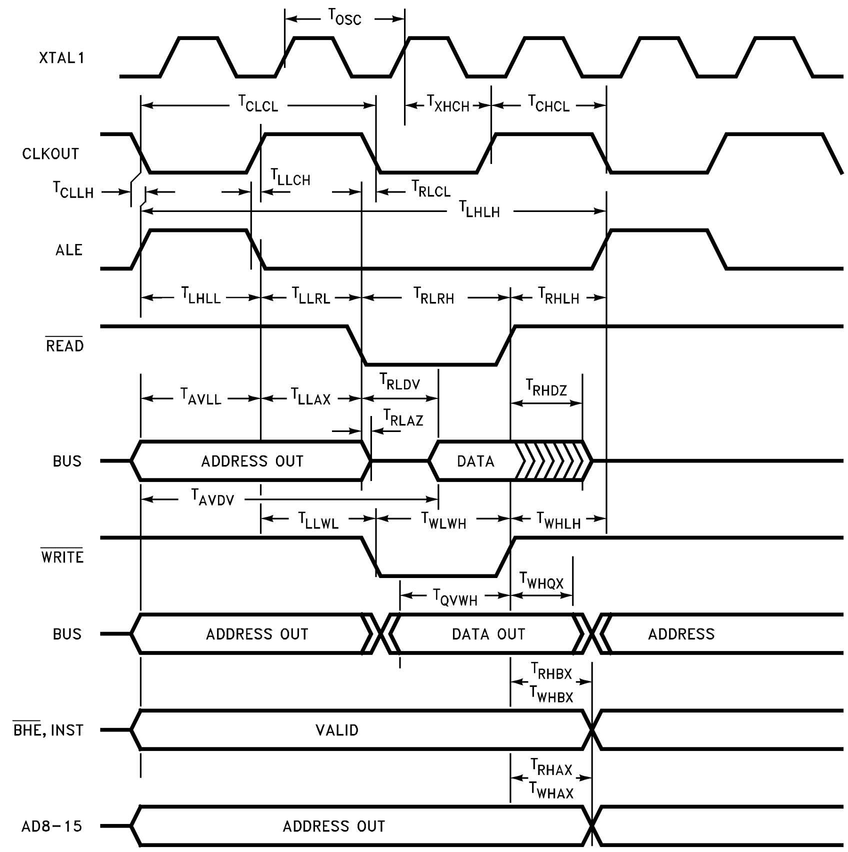
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The 87C196KB will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 12 MHz	3.5	12.0	MHz	(Note 2)
F_{XTAL}	Frequency on XTAL1 16 MHz	3.5	16.0	MHz	(Note 2)
T_{OSC}	1/F $_{XTAL}$ 12 MHz	83.3	286	ns	
T_{OSC}	1/F $_{XTAL}$ 16 MHz	62.5	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	+10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{RHBX}	$\overline{BHE}$, INST HOLD after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8±15 hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8±15 hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Assuming back-to-back bus cycles.
2. Testing performed at 3.5 MHz, however, the device is static by design and will typically operate below 1 Hz.
3. When using wait states, all 2 T_{OSC} + n where n = number of wait states.

System Bus Timings



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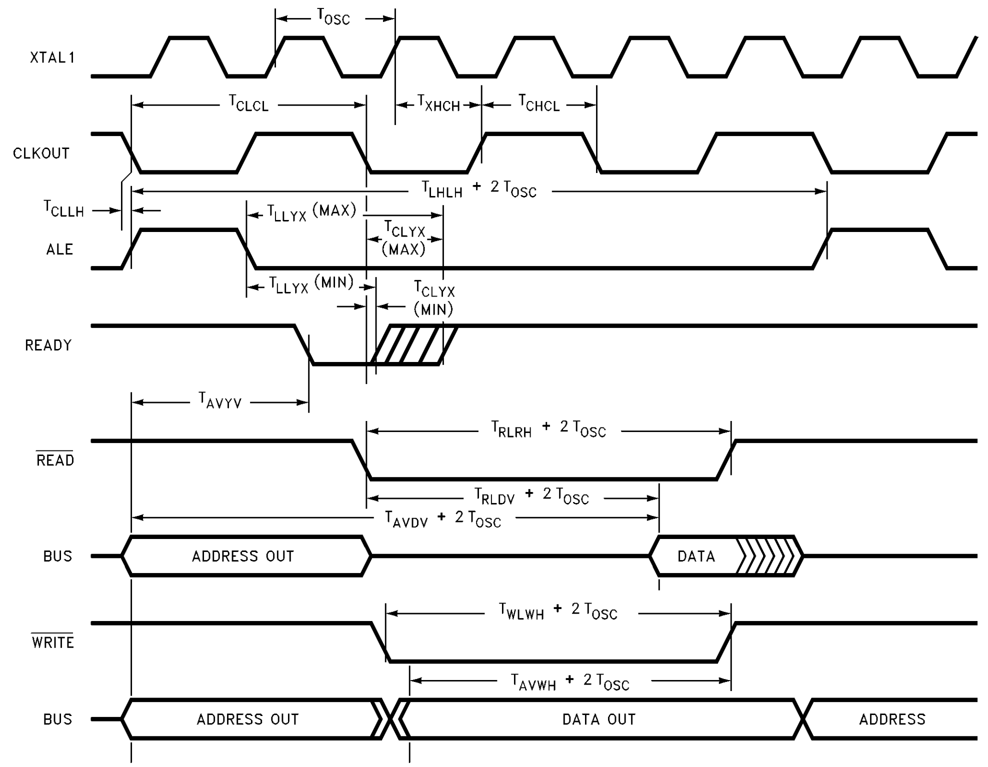
READY Timings (One Wait State)



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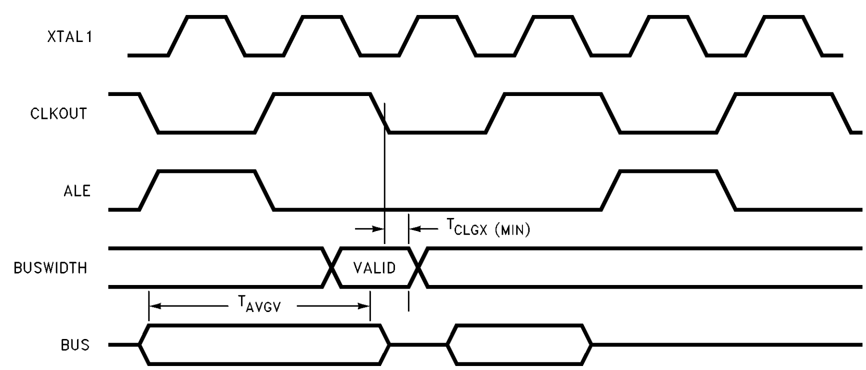
Buswidth Bus Timings



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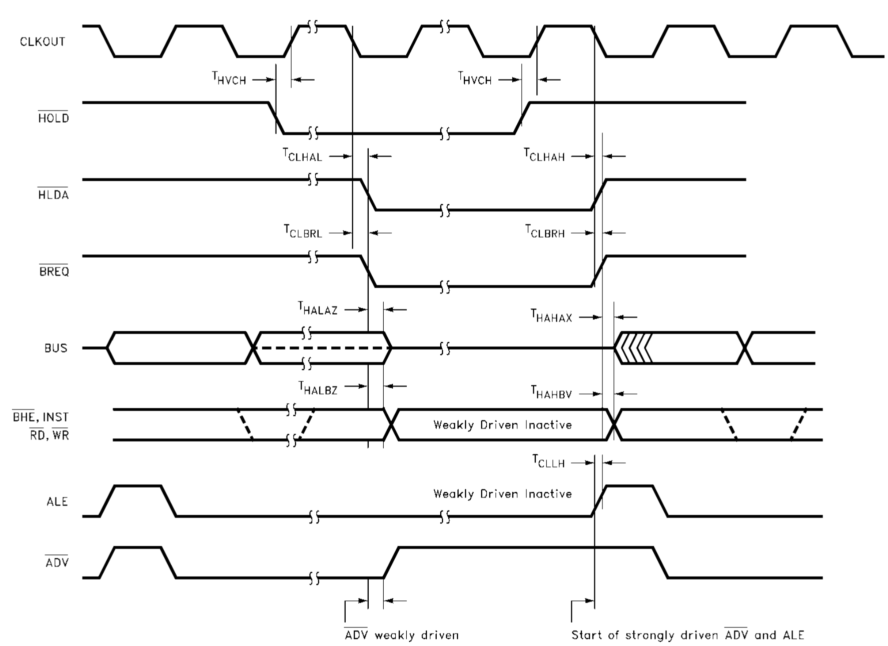
HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low		15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low		15	ns	
T_{HALAZ}	HLDA Low to Address Float		10	ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Float		10	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHAV}	HLDA High to Address Valid	0		ns	
T_{HAHBX}	HLDA High to BHE, INST, RD, WR No Longer Float	−20		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	0		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

Maximum Hold Latency

Bus Cycle Type	Latency
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External	4.5 States

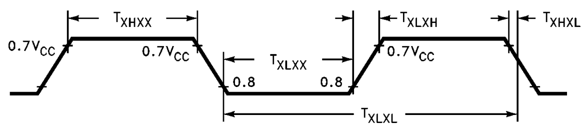


270909±9

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency 12 MHz	3.5	12.0	MHz
$1/T_{XLXL}$	Oscillator Frequency 16 MHz	3.5	16	MHz
T_{XLXL}	Oscillator Period 12 MHz	83.3	286	ns
T_{XLXL}	Oscillator Period 16 MHz	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

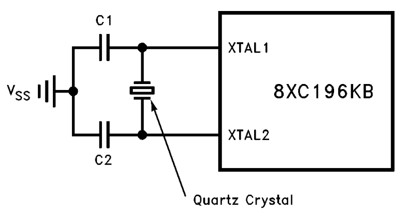
EXTERNAL CLOCK DRIVE WAVEFORMS



270909±10

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

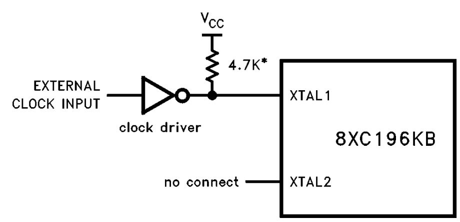
EXTERNAL CRYSTAL CONNECTIONS



270909±11

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

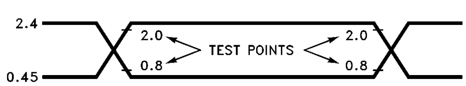
EXTERNAL CLOCK CONNECTIONS



270909±12

* Required if open-collector TTL driver used
Not needed if CMOS driver is used.

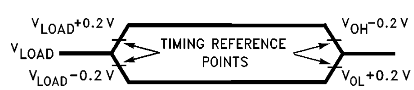
AC TESTING INPUT, OUTPUT WAVEFORMS



270909±13

AC Testing inputs are driven at 2.4V for a Logic ``1'' and 0.45V for a Logic ``0'' Timing measurements are made at 2.0V for a Logic ``1'' and 0.8V for a Logic ``0''.

FLOAT WAVEFORMS



270909±14

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs; $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by ``T'' for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

Signals:

H - High	A - Address	G - Buswidth	R - $\overline{RD}$
L - Low	B - $\overline{BHE}$	H - $\overline{HOLD}$	W - $\overline{WR}/\overline{WRH}/\overline{WRL}$
V - Valid	BR - $\overline{BREQ}$	HA - $\overline{HLDA}$	X - XTAL1
X - No Longer Valid	C - CLKOUT	L - ALE/$\overline{ADV}$	Y - READY
Z - Floating	D - DATA IN	Q - DATA OUT	

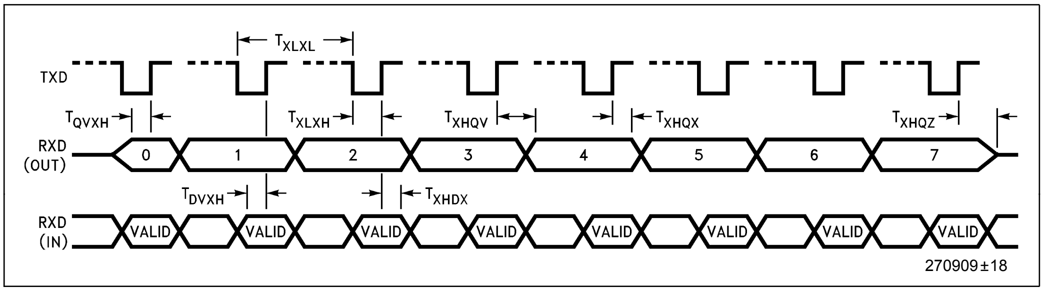
AC CHARACTERISTICS-SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING-SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		2 T_{OSC}	ns

WAVEFORM-SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT WAVEFORM-SHIFT REGISTER MODE (MODE 0)



10-BIT A/D CHARACTERISTICS

At a clock speed of 6 MHz or less, the clock prescaler should be disabled. This is accomplished by setting IOC2.4 = 1.

At higher frequencies (greater than 6 MHz) the clock prescaler should be enabled (IOC2.4 = 0) to allow the comparator to settle.

The table below shows two different clock speeds and their corresponding A/D conversion and sample times.

State times are calculated as follows:

$$\text{state time} = \frac{2}{\text{XTAL1}}$$

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for definition of A/D terms.

Example Sample and Conversion Times

A/D Clock Prescaler	Clock Speed (MHz)	Sample Time (States)	Sample Time at Clock Speed (μs)	Conversion Time (States)	Conversion Time at Clock Speed (μs)
IOC2.4 = 0 → ON	16	15	1.875	156.5	19.6
IOC2.4 = 1 → OFF	6	8	2.667	89.5	29.8

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units *	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An ``LSB'', as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

OTPROM SPECIFICATIONS

OTPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages During Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **12 MHz**	6.0	12.0	MHz
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

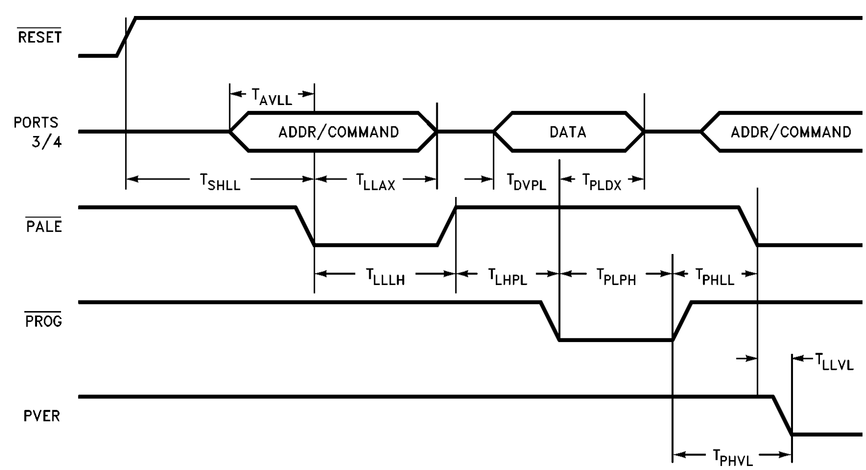
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

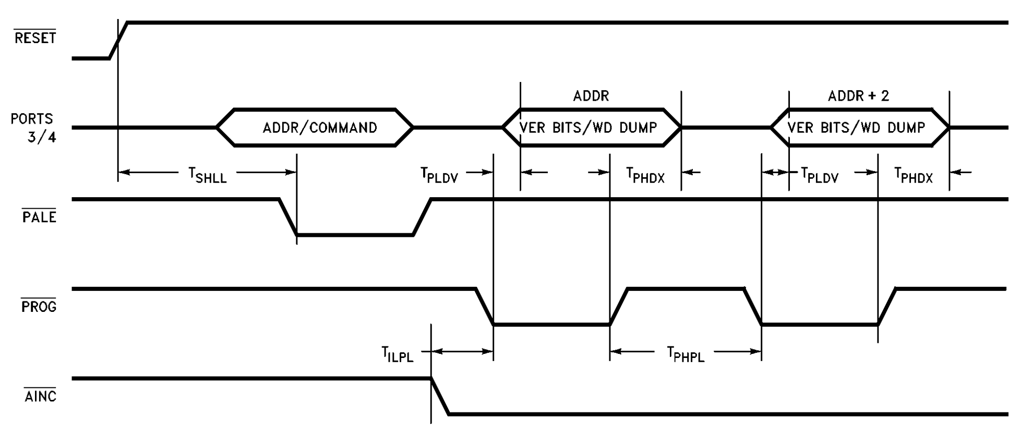
OTPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



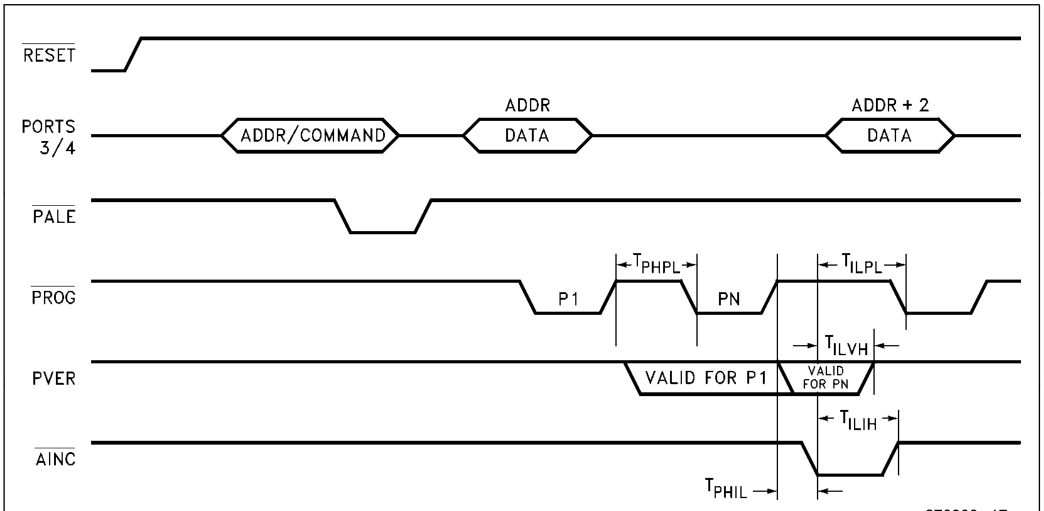
270909±15

SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



270909±16

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



270909±17

FUNCTIONAL DEVIATIONS

Devices marked with an ''E'', ''F'' or ''G'' have the following errata.

1. Missed Interrupt on P0.7, EXTINT

Interrupts occurring on P0.7 could be missed since the INT_PEND EXTINT bit may not be set. See techbit MC0893.

2. HSI_ MODE Divide-by-Eight

REVISION HISTORY

This data sheet (270909-006) is valid for devices with an ''E'', ''F'' or ''G'' at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270909-007) and (270909-006).

1. Package prefix variables have changed. These variables are now indicated by "**x**".

The following differences exist between data sheet 270909-006 and 270909-005.

1. Removed ''Word Addressable Only'' from Port 3 and 4 in Table 2.
2. Removed ICC1, active mode current at 3.5 MHz. This specification is not longer required.
3. Removed TLLYV and TLLGV from waveform diagrams.
4. The HSI errata and CMPL with R0 were removed as this is now considered normal operation.
5. The HSI_MODE divide-by-eight errata was added to the known errata section.

The following differences exist between this data sheet (270909-005) and (270909-004).

1. I_{TL} MAX was − 650 µA (270909-004). Now I_{TL} MAX is − 800 µA (270909-005).
2. I_{IL2} was named I_{IL1} (270909-004). Now I_{IL2} is correctly named (270909-005).
3. I_{IL1} was omitted (270909-004). I_{IL1} MAX was added. I_{IL1} MAX is − 850 µA (270909-005).
4. T_{LLYV} and T_{LLGV} (270909-004) were removed. These timings are not required in high-speed system designs.
5. An errata was added to the known errata section. There is a possibility to miss an external interrupt on P0.7 EXTINT.

The following differences exist between this data sheet (270909-004) and (270909-003).

1. The ROM (80C196KB), and ROMless (83C196KB) were combined with this data sheet resulting in no specification differences.
2. The description of the prescalar bit for the A/D has been enhanced.
3. T_{HAHBV}MIN was − 15 ns (270909-003). Now T_{HAHBV}MIN is − 20 ns (270909-004).
4. T_{XHQZ}MAX was 1 TOSC (270909-003). Now T_{XHQZ}MAX is 2 TOSC (270909-004). This should have no impact on designs using synchronous serial mode 0.
5. The change indicators for the 80C196KB are ''E'', ''F'' and ''G''. Previously there was only one change indicator ''E''. The change indicator is used for tracking purposes. The change indicator is the last character in the FPO number. The FPO number is the second line on the top side of the device.

The following differences exist between (-003) and version (-002).

1. The 12 MHz and 16 MHz devices were combined in this data sheet. The 87C196KB 12 MHz only data sheet (272035-001) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed.
3. The -002 version of this data sheet was valid for devices marked with a ``B'' or a ``D'' at the end of the top side tracking number.
4. The OSCILLATOR errata was removed.
5. An errata was not documented in the -002 data sheet for devices marked with a ``B'' or a ``D''. This is the DIVIDE DURING HOLD/READY errata. When HOLD or READY is active and DIV/DIVB is the last instruction in the queue, the divide result may be incorrect.
6. T_{XCH} was changed from Min = 40 ns to Min = 20 ns.
7. T_{RLCL} was changed from Min = 5 ns to Min = 4 ns.
9. I_{IL1} was changed from Max = −6 mA to Max = −7 mA.
10. T_{HAHBV} was changed from Min = −10 ns to Min = −15 ns.

Differences between the -002 and -001 data sheets.

1. The -001 version of this data sheet was valid for devices marked with a ``C'' at the end of the top side tracking number.
2. Added 64L SDIP and 80L QFP packages.
3. Added IIH1.
4. Changed T_{CHWH} Min from − 10 ns to − 5 ns.
5. Changed T_{CHWH} Max from + 10 ns to + 15 ns.
6. Changed T_{WLWH} Min from T_{OSC} − 20 ns to T_{OSC} − 15 ns.
7. Changed T_{WHQX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
8. Changed T_{WHLH} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
9. Changed T_{WHLH} Max from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
10. Changed T_{WHBX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
11. Changed T_{HVCH} Min from 85 ns to 55 ns.
12. Remove T_{HVCH} Max.
13. Changed T_{CLHAL} Min from − 10 ns to − 15 ns.
14. Changed T_{CLHAL} Max from 20 ns to 15 ns.
15. Changed T_{CLBRL} Min from − 10 ns to − 15 ns.
16. Changed T_{CLBRL} Max from 20 ns to 15 ns.
17. Changed T_{HAHAX} Min from − 10 ns to − 15 ns.
18. Added HSI description to Functional Deviations.
19. Added Oscillator description to Functional Deviations.